مشروع مادة الـ Digital Logic Design

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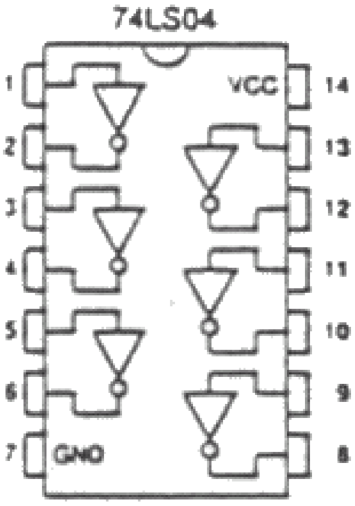
فترة الصيف لعام 2008

الأكاديمية العربية للعلوم و التكنولوجيا

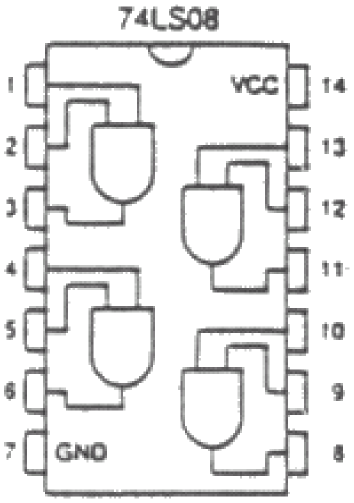
2-Bit Comparator

Integrated Circuits Used

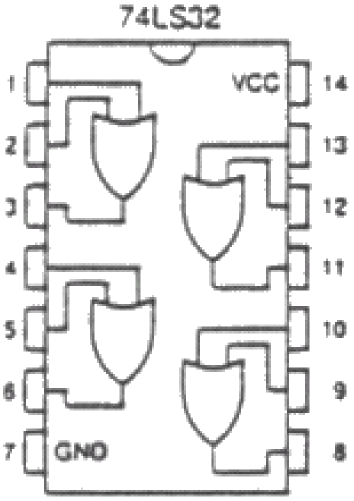
الدوائر التكاملية المستخدمة



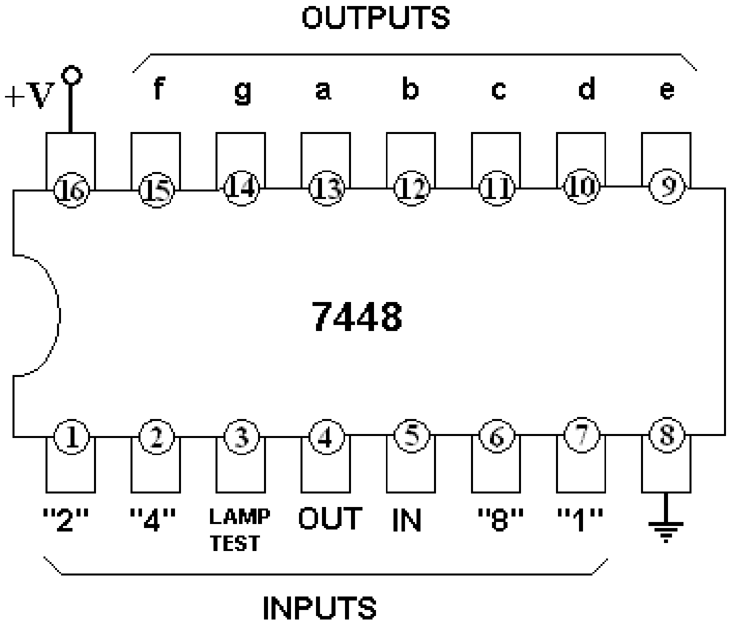
Inverter



AND



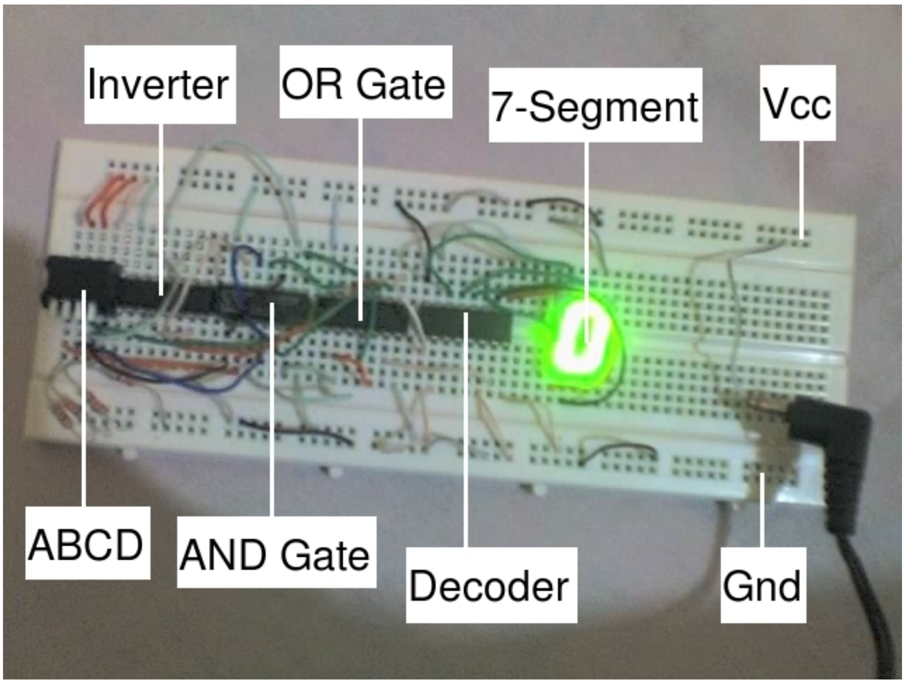
OR

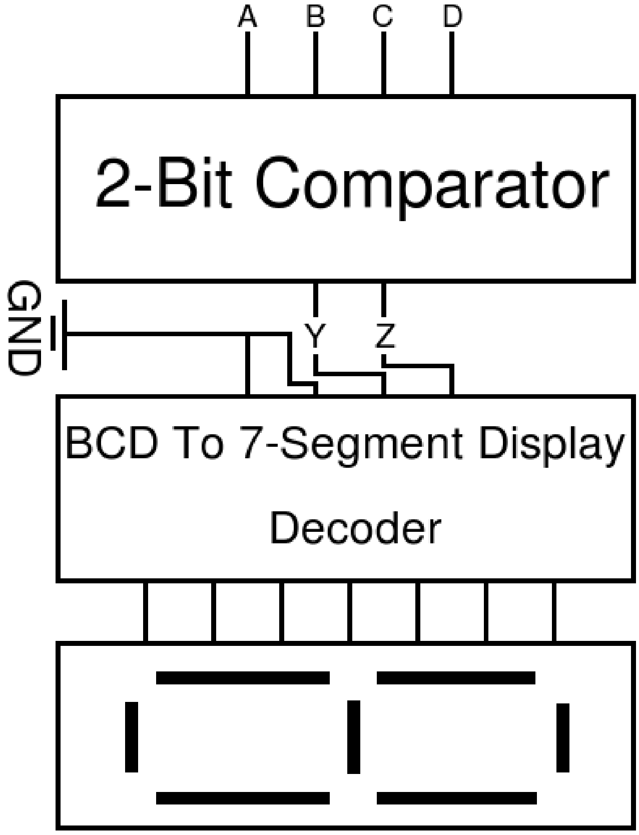


BCD To 7 Segment

Design Components

مكونات التصميم





We input two 2-bit numbers to the Comparator.
The Comparator's output is the biggest number.
Z is the first Bit (LSB) , Y is the Second Bit.
We put y and z and two zeros into the decoder then from the Decoder to The 7-Segment Display.

Comparator's Truth Table

A	B	C	D	Y	Z
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

K-Maps

Y

0	**0**	**1**	**1**
0	**0**	**1**	**1**
1	**1**	**1**	**1**
1	**1**	**1**	**1**

$Y = A + C$

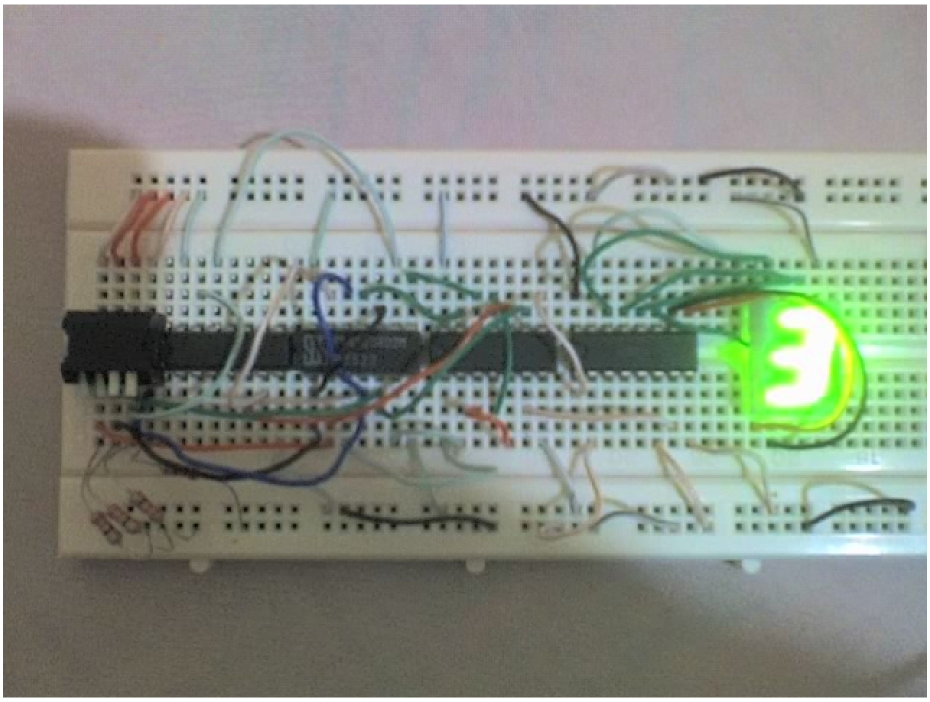
Z

0	**1**	**1**	**0**
1	**1**	**1**	**0**
1	**1**	**1**	**1**
0	**0**	**1**	**0**

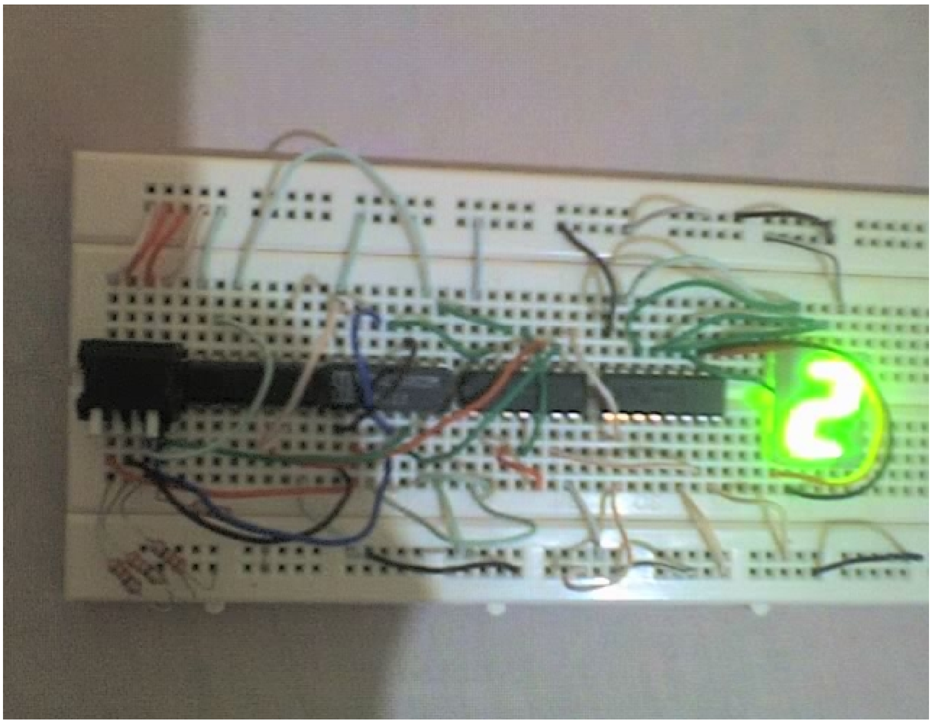
$Z = AB + CD + \overline{A}D + B\overline{C}$

At Runtime

أثناء التشغيل



The First Number = $(11)_2 = (3)_{10}$
The Second Number = $(00)_2 = (0)_{10}$



The First Number = $(01)_2 = (1)_{10}$
The Second Number = $(10)_2 = (2)_{10}$